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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,783	06/22/2000	Toshiharu Furukawa	BU9-99-197	7947

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/599,783	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-6,8,11,12,14,19-21,26-28,30 and 32-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-6,8,11,12,14,19-21,26-28,30 and 32-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The addition of claims 33-43 as set forth in paper file on 03/04/2004 is acknowledged.

2. Claims 3-6, 8, 11, 12, 14, 19-21, 26-28, 30, and 32-43 are pending in the application.

Claim Objections

3. Claim 3 is objected to because of the following informalities: in claim 3, line 1, applicants recite, "...A method for etching a semiconductor substrate using a germanium hardmask...". However, in claim 3, lines 24-25 specifically excludes etching the substrate. It is suggested that in claim 3, line 1, where applicants recite, "...A method for etching a semiconductor substrate using a germanium hardmask...", should recite -- A method for etching a dielectric layer over a semiconductor substrate using a germanium hardmask --.

4. Also, claims 3, 11, 19, 26 and 32 are objected to because of the following informalities: in claim 3, line 12, where applicants recite "photo resist layer", should recite, --photolithography image--; in claim 11, line 11, where applicants recite "photo resist layer", should recite, --photolithography image--; in claim 19, line 11, where applicants recite "photo resist layer" should recite, --photolithography image--; in claim 26, line 9, where applicants recite "photo resist layer" should recite –photolithography image--; and in claim 32, line 11, where applicants recite "photo resist layer", should recite, --photolithography image--.

5. Furthermore, claims 5, 19 and 26 are objected to because of the following informalities: in reference to claims 5, 19 and 26, applicants recite, "removing the layer of germanium oxide after performing the step of oxidizing the layer of metallic germanium". However, the layer of germanium oxide is already oxidized at the moment of its removal.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 6, 21,28, 33, 34, and 36-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 recites "...method as claimed in claim 3, wherein the step of oxidizing...". However, such oxidizing step is not found in claim 3. Therefore, there is insufficient antecedent basis for this limitation. Also, claims 6, 21,28, 33, 34, and 36-41 recite an oxidizing step at "elevated temperature. This renders the claims indefinite since there is not description of temperature ranges to which the term elevated encompasses. If applicants wish to establish a particular temperature range, it must be clearly recited.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 8, 32, 35 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shoji et al. (U.S. 5,928,965) in view of Subramanian et al. (U.S. 6,060,380), Avanzino et al. (U.S. 6,121,150), Koch et al. (U.S. 5,413,884) and Ke et al. (U.S. 2002/0066531 A1).

In reference to claims 3, 32, 35 and 43, Shoji et al. Fig.1) in a related method to form a trench in a substrate (101) teach forming a dielectric stack (102, 103, 104) comprising a plurality of dielectric layers including silicon oxide over said semiconductor substrate (101); forming a photo resist (105) over said dielectric stack (102, 103, 104); pattern on the photo resist; selectively etching said dielectric stack (102, 103, 104), thus forming a dielectric hardmask; removing said photoresist prior to etching said substrate (101); and selectively etching the said semiconductor substrate (101) through the opening in said dielectric hardmask (column 3, line 43 – column 4, line 12).

Shoji et al. fail to teach depositing a hardmask over said dielectric stack; forming the photoresist over the hard mask layer; exposing the photoresist layer to light and developing the exposed photo resist layer to form a photolithography image; etching the layer of hardmask through the photolithography image; and removing the photolithography image prior to selectively etching the dielectric stack. However, Subramanian et al. (Figs.4A-4G) in a method to form interconnects teach depositing a dielectric stack (302, 112, 304, 118) comprising an interlevel dielectric over a substrate (106); forming a hardmask layer (306) over said dielectric stack (302, 112, 304, 118); forming a photo resist layer (308) over said hardmask layer (306); exposing the photo

resist layer (308) to light and developing the exposed photo resist to form a photolithography image; etching the hardmask layer (306) through the photolithography image; removing said photolithography image; and selectively etching the dielectric layer stack (302, 112, 304, 118) through said hardmask layer (306) with the hardmask layer as a topmost layer; and removing said hardmask layer (306) before further processing of the device (column 3, line 37 – column 4, line 64).

Furthermore, according to Avanzino et al., typical materials used as interlevel dielectrics for the fabrication of interconnects include silicon oxide and silicon nitride, among others (column 9, lines 35 – 51). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Shoji et al. and Subramanian et al. to enable the patterning step of Shoji et al. according to the teachings of Subramanian for the further advantage of improving alignment of said patterning of said dielectric stack (column 4, line 49 – column 5, line 23), and because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed patterning step of Shoji et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Shoji et al. and Subramanian et al. fail to teach depositing a layer of metallic germanium over the dielectric stack; etching the layer of metallic germanium through the photolithography image, forming a germanium hardmask; and selectively etching said dielectric stack through said germanium hardmask as a top most layer to form an opening in the dielectric stack.

However, Koch et al. (Figs.7-11) in a related method to etch a dielectric stack teach the steps of depositing a layer of metallic germanium (44) over a dielectric stack (32, 42), comprising quartz; patterning the layer of metallic germanium (44) to form the germanium hard mask as a top most layer over the dielectric stack (32, 42) by depositing a photo resist layer (46) over the layer of metallic germanium (44), patterning the photo resist layer (46) to form a photolithography image (50) and etching the layer of metallic germanium (44) through the photolithography image (50); selectively etching the dielectric stack (32, 42) through the germanium hard mask (44) as a to form an opening in the dielectric layer (32, 42); striping away the layer of metallic germanium (column 5, line 26 – column 6, line 27).

Furthermore, according to Ke et al., quartz if chemically identical to silicon oxide ([0045]). Therefore, it would have been within the scope of one of ordinary skill in the art to combine the teachings of Shoji et al. and Subramanian et al with Koch et al. to enable the patterning the dielectric layer of Shoji et al. and Subramanian et al. using the metallic germanium hardmask according to the teachings of Koch et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed patterning step of Shoji et al. and Subramanian et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

In reference to claim 8, the combined teachings of Shoji et al., Subramanian et al., Avanzino et al., Koch et al. and Ke et al. teach wherein the dielectric stack comprises a plurality of dielectric layer and further comprises the steps of forming a pad

oxide layer; depositing a nitride layer; and depositing a mask oxide layer (Shoji et al., column 3, lines 43 – 57).

Shoji et al., Subramanian et al., Avanzino et al., Koch et al. and Ke et al. fail to teach forming said pad oxide layer, said nitride layer and said mask oxide layer with a thickness between approximately 5 nm and approximately 30 nm, between approximately 50 nm and approximately 300 nm, and between approximately 800 nm and approximately 3,000 nm, respectively. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

10. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shoji et al. ('965) in view of Subramanian et al. ('380), Avanzino et al. (150), Koch et al.

('884) and Ke et al. ('531 A1) as applied to claims 3, 8, 32, 35 and 43 above, and further in view of Howe et al. (U.S. 6,210,988 B1).

The combined teachings of Shoji et al., Subramanian et al., Avanzino et al., Koch et al. and Ke et al. substantially teach all aspects of the invention but fail to teach stripping away the germanium layer from the dielectric stack by oxidizing the germanium layer, transforming it to germanium oxide and rinsing the germanium oxide layer with water. However, Howe et al. in a related method to form sacrificial films teach removing a germanium layer (405) by oxidizing said layer and stripping away said oxidized germanium layer with a solution comprising water (column 2, lines 40-50, column 3, lines 36-51 and column 5, lines 36-53). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Shoji et al., Subramanian et al., Avanzino et al., Koch et al. and Ke et al. with Howe et al. to enable the stripping of the germanium layer step of Shoji et al., Subramanian et al., Avanzino et al., Koch et al. and Ke et al. to be performed according to the teachings of How et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed stripping step of Shoji et al., Subramanian et al., Avanzino et al., Koch et al. and Ke et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07), and furthermore, since this would allow the removal of said layer without any damage to the rest of the device (column 7, lines 21-31).

11. Claims 11, 14, 19, 26, 30 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shoji et al. ('965) in view of Subramanian et al. ('380), Avanzino et al. ('150), Koch et al. ('884), Ke et al. ('531 A1) and Howe et al. ('988 B1).

In reference to claims 11, 19, 26 and 42, Shoji et al. Fig.1) in a method to form isolation regions for LSI devices teach forming a dielectric stack (102, 103, 104) comprising a plurality of dielectric layers including silicon oxide over a semiconductor substrate (101); forming a photo resist (105) over said dielectric stack (102, 103, 104); pattern on the photo resist; selectively etching said dielectric stack (102, 103, 104), thus forming a dielectric hardmask; removing said photoresist prior to etching said substrate (101); and selectively etching the said semiconductor substrate (101) through the opening in said dielectric hardmask (column 3, line 43 – column 4, line 12).

Shoji et al. fail to teach depositing a hardmask over said dielectric stack; forming the photoresist over the hard mask layer; exposing the photoresist layer to light and developing the exposed photo resist layer to form a photolithography image; etching the layer of hardmask through the photolithography image; and removing the photolithography image prior to selectively etching the dielectric stack. However, Subramanian et al. (Figs.4A-4G) in a method to form interconnects teach depositing a dielectric stack (302, 112, 304, 118) comprising an interlevel dielectric over a substrate (106); forming a hardmask layer (306) over said dielectric stack (302, 112, 304, 118); forming a photo resist layer (308) over said hardmask layer (306); exposing the photo resist layer (308) to light and developing the exposed photo resist to form a photolithography image; etching the hardmask layer (306) through the photolithography

image; removing said photolithography image; and selectively etching the dielectric layer stack (302, 112, 304, 118) through said hardmask layer (306) with the hardmask layer as a topmost layer; and removing said hardmask layer (306) before further processing of the device (column 3, line 37 – column 4, line 64).

Furthermore, according to Avanzino et al., typical materials used as interlevel dielectrics for the fabrication of interconnects include silicon oxide and silicon nitride, among others (column 9, lines 35 – 51). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Shoji et al. and Subramanian et al. to enable the patterning step of Shoji et al. according to the teachings of Subramanian for the further advantage of improving alignment of said patterning of said dielectric stack (column 4, line 49 – column 5, line 23), and because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed patterning step of Shoji et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Shoji et al. and Subramanian et al. fail to teach depositing a layer of metallic germanium over the dielectric stack; etching the layer of metallic germanium through the photolithography image, forming a germanium hardmask; and selectively etching said dielectric stack through said germanium hardmask as a top most layer to form an opening in the dielectric stack. However, Koch et al. (Figs.7-11) in a related method to etch a dielectric stack teach the steps of depositing a layer of metallic germanium (44) over a dielectric stack (32, 42), comprising

quartz; patterning the layer of metallic germanium (44) to form the germanium hard mask as a top most layer over the dielectric stack (32, 42) by depositing a photo resist layer (46) over the layer of metallic germanium (44), patterning the photo resist layer (46) to form a photolithography image (50) and etching the layer of metallic germanium (44) through the photolithography image (50); selectively etching the dielectric stack (32, 42) through the germanium hard mask (44) as a to form an opening in the dielectric layer (32, 42); striping away the layer of metallic germanium (column 5, line 26 – column 6, line 27).

Furthermore, according to Ke et al., quartz if chemically identical to silicon oxide ([0045]). Therefore, it would have been within the scope of one of ordinary skill in the art to combine the teachings of Shoji et al. and Subramanian et al with Koch et al. to enable the patterning the dielectric layer of Shoji et al. and Subramanian et al. using the metallic germanium hardmask according to the teachings of Koch et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed patterning step of Shoji et al. and Subramanian et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Shoji et al., Subramanian et al. and Koch et al. fail to teach stripping away the germanium layer from the dielectric stack by oxidizing the germanium layer, transforming it to germanium oxide and rinsing the germanium oxide layer with water. However, Howe et al. in a related method to form sacrificial films teach removing a germanium layer (405) by oxidizing said layer and stripping away said

oxidized germanium layer with a solution comprising water (column 2, lines 40-50, column 3, lines 36-51 and column 5, lines 36-53). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Shoji et al., Subramanian et al. and Koch et al. with Howe et al. to enable the stripping of the germanium layer step of Shoji et al., Subramanian et al., and Koch et al. to be performed according to the teachings of Howe et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed stripping step of Shoji et al., Subramanian et al. and Koch et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07), and furthermore, since this would allow the removal of said layer without any damage to the rest of the device (column 7, lines 21-31).

Still, the prior art of record fail to teach forming the germanium layer with a thickness equal or greater than approximately 40 nm. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose,

220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In reference to claims 14 and 30, the combined teachings of Shoji et al., Subramanian et al., Avanzino et al., Koch et al. and Ke et al. teach wherein the dielectric stack comprises a plurality of dielectric layer and further comprises the steps of forming a pad oxide layer; depositing a nitride layer; and depositing a mask oxide layer (Shoji et al., column 3, lines 43 – 57).

Shoji et al., Subramanian et al., Avanzino et al., Koch et al. and Ke et al. fail to teach forming said pad oxide layer, said nitride layer and said mask oxide layer with a thickness between approximately 5 nm and approximately 30 nm, between approximately 50 nm and approximately 300 nm, and between approximately 800 nm and approximately 3,000 nm, respectively. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d

459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Response to Arguments

12. Applicant's arguments with respect to claims 3-6, 8, 11, 12, 14, 19-21, 26-28, 30, and 32-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is 571-272-2800. See MPEP 203.08.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

George Fourson
Primary Examiner

Julio J. Maldonado
May 10, 2004